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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,584	12/09/2003	Jochen C. Beintner	YOR920030380US1	3887

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,584	BEINTNER ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4,6,7 and 13-22 is/are rejected.

7)☒ Claim(s) 5,8-12 and 23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 19-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (US 2004/0036126 A1).

With reference to Figs. 5D-5J, the reference teaches every element of the claimed structure in that it discloses an integrated circuit comprising at least one FinFET comprising:

a set of at least one semiconducting fin(s) **520** on a substrate (Fig. 5D);

said set of fins having a gate insulator **526** separating a body region thereof from a self-aligned gate **530** intersecting said set of fins and defining said body region in said fins below said gate (Fig. 5E and para. [0041], [0042]);

a separation layer of insulator **550** covering said gate and exposing said set of fins (Fig. 5G); and

source and drain regions **560** in said fins, self-aligned to said gate and separated from said gate by said insulator layer **550** (Fig. 5H).

Note that, the process of which the gate **530** and the separation layer **550** are formed carries no patentable weight in a product claim because it is well established that the patentability of a product does not depend on its method of production. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

For claims 20 and 22, see S/D material **560** of silicon in Fig. 5H and silicide **570** in Fig. 5J, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 7, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al as above in view of Hu et al. (US 6,413,802).

With reference to Figs. 5D-5J, Chau teaches a method of forming a FinFET, comprising the steps of:

forming a set of at least one semiconducting fin **520** on a substrate (Fig. 5D);

forming a gate insulator **526** on said set of fins (Fig. 5E and para.[0041];

depositing a layer of gate material over said set of fins;

etching said gate material to form a gate **530** intersecting said set of fins and defining a body region in said fins below said gate (Fig. 5E and para.[0042]);

depositing a conformal layer **550** of insulator enclosing said gate;

performing an anisotropic etch of said conformal layer, thereby exposing said set of fins while said gate remains covered by said conformal layer of insulator (Fig. 5G and para. [0046]; and

forming source and drain regions **560** in said fins, separated from said gate by said conformal layer of insulator (Fig. 5I).

The difference between Chau and the claims is that while Chau teaches patterning the gate material by well-known photolithography and etching techniques to form the gate electrode **530** (para. [0042]), the claims call for the formation of a hardmask on the gate material and then etching the gate material outside said hardmask thereby forming a gate electrode. However, Hu teaches a conventional photolithography in which a hardmask pattern is used as an etching mask for patterning a gate electrode (Fig. 2D). Thus, it would have been obvious to one of ordinary skill in the art to form the gate electrode **530** by etching the gate material using a patterned hard mask as suggested by Hu because such lithography process is commonly practiced in the art, and the application of a known process to make the same would have been within the level of one skilled in the art.

For claim 2, see S/D material of silicon **560** over a set of at least two fins in Fig. 5H.

For claims 4, 7, and 17, see Fig. 5J and paragraph [0050] for the formation of silicide layers on exposed silicon in the fins and in an upper portion of the gate.

5. Claims 1-4, 6-7, 13, and 15-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al (US 6,252,284) in view of Chau et al. cited above.

With reference to Figs. 7A-14, Muller teaches a method of forming a FinFET, comprising the steps of:

forming a set of at least one semiconducting fin **4** on a substrate;

forming a gate insulator **12** on said set of fins (Fig. 7A);

depositing a layer of gate material **21** over said set of fins;

forming a hardmask **22** on said gate material extending perpendicular to said set of fins and having a hardmask thickness (Fig. 8A);

etching said gate material outside said hardmask down to said substrate, thereby forming a gate intersecting said set of fins and defining a body region in said fins below said gate (Figs. 9B and 14);

forming spacers **23** exposing said set of fins and covering said gate (Figs. 10B and 14); and

forming source and drain regions **25** in said fins, separated from said gate by said spacers **23**.

Muller differs from the claims in not disclosing the process of which the spacers **23** are formed. Chau teaches a method for forming a FinFET device in which spacers on sidewalls of a gate electrode are fabricated by depositing a conformal layer of insulator enclosing the gate and then performing an anisotropic etch of the conformal layer, thereby forming the spacers (para. [0046], [0047]). Thus, it would have been obvious to of one ordinary skill in the art to form the spacers **23** by depositing a conformal layer followed by an anisotropic etch as taught by Chau because such process of forming spacers is commonly practiced in the art, and the application of a known process to make the same would have been within the level of one skilled in the art.

For claims 2 and its dependent claims, Muller differs from the claims in that while Muller teaches a FinFET having a single fin, the claims call for a FinFET having at least two fins. However, Chau in Figs. 5A-5J teaches a FinFET having a plurality of fins. It would have been obvious to of one ordinary skill in the art to modify Muller's process by forming a plurality of fins for the FinFET as suggested by Chau because a FinFET having a plurality of fins would produce higher source/drain current than that of a FinFET with one fin due to the existence of multiple channels of the former device.

For claim 3, see Fig. 12B and related text for the steps of recessing S/D material and forming S/D contacts.

For claims 4, 7, 15-18, see silicide layers 26 and 28 of Fig. 13B.

For claims 6 and 13, see the remaining hardmask 22 in Fig. 10B.

For device claims 19-22, the combined process described above would produce the structure as claimed.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 is confusing. Claim 14 when read back to its based claims (i.e., claims 13 and then 1) would result in a claim having duplicate limitations. Clarification is required.

Allowable Subject Matter

8. Claims 5, 8-12, and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

Prior art of record does not teach or suggest the limitation regarding the formation of a blocking material and a second conformal insulating layer in a manner as recited in claims 5 and 8.

For device claim 23, the prior art does not teach or suggest the claimed FinFET having a first subset of N-type FinFETs that has a first thickness of said separation layer and a second subset of P-type FinFETs that has a second thickness of separation layer, said second thickness being greater than said first thickness.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

10/05/04